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| 08/327,887 | 10/24/94 | KIM | S 9983,3US01 |
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D1M1/1108

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| 1107 | 26 |

DATE MAILED: 11/08/96

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on 10/19/96

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

- ☒ Claim(s) 1, 2, 7-9 is/are pending in the application.
Of the above, claim(s) _____ is/are withdrawn from consideration.
- ☐ Claim(s) _____ is/are allowed.
- ☒ Claim(s) 1, 2, 7-9 is/are rejected.
- ☐ Claim(s) _____ is/are objected to.
- ☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

- ☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- ☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

- ☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
- ☐ received.
- ☐ received in Application No. (Series Code/Serial Number) _____
- ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- ☒ Notice of Reference Cited, PTO-892
- ☐ Information Disclosure Statement(s), PTO-1449, Paper No(s) _____
- ☐ Interview Summary, PTO-413
- ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948
- ☐ Notice of Informal Patent Application, PTO-152

-SEE OFFICE ACTION ON THE FOLLOWING PAGES-

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The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Since this application is eligible for the transitional procedure of 37 CFR 1.129(a), and the fee set forth in 37 CFR 1.17(r) has been timely paid, the finality of the previous Office action is hereby withdrawn pursuant to 37 CFR 1.129(a). Applicant's first submission after final filed on 10/15/96 has been entered.

Claim 9 is rejected under 35 U.S.C. § 103 as being unpatentable over the admitted prior art in view of Gutierrez [US 5,056,749].

The admitted prior art teaches providing a silicon substrate (10); forming a field oxide (3), junction layer (2), and polysilicon gate electrode (5); forming a first insulating layer (6) over the structure; forming a patterned polysilicon conductive layer (7) on the first insulating layer; forming a second insulating layer (8) over the first; forming holes in the first and second insulating film to the gate and junction followed by filling the holes with CVD tungsten (9) (Figures 1A, 1B). The admitted prior art doesn't teach filling the first holes with selective CVD tungsten prior to forming the second insulating layer or a second step of forming selective CVD tungsten in the second insulating layer via holes.

Gutierrez teaches forming a field oxide region (122) a junction layer (116) and a patterned polysilicon conductor (114) over a semiconductor substrate (140), forming an insulating layer

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(124 or 230), forming contact holes (110, 112) to the poly conductor and the junction layer, selectively forming tungsten (226, 228) in the contact holes, forming a second insulating layer (232) on the first insulating layer (Figures 7 and 8, col 4, line 35-col 5, line 18), and repeating the process to form contact vias (224) and metal interconnection lines (220,216) (col 5, lines 18-21), where the process doesn't require planarization and can be performed on an uneven surface (col 5, lines 39-53). It can be seen from the Figures that the holes are of a substantially even depth in a given insulating layer. Gutierrez teaches forming the polysilicon conductor (114) which extends over a region isolated by field oxide regions and teaches the device may be an NMOS (Figure 7, col 4, lines 54-65). Therefore it seems that the polysilicon (114) may be a gate electrode but this is not completely clear.

It would have been obvious for one with ordinary skill in the art in the process of the admitted prior art to have filled the holes in the first insulating layer with selective CVD tungsten prior to forming the second insulating layer and a second step of forming selective CVD tungsten in the second insulating layer via holes for the advantages taught by Gutierrez.

It is noted that claim 9 requires that filling contact holes with a first metal by "one single step". However, this language does not preclude switching source gases during the single step of filling the hole. The specification (page 3 for instance) discloses only that a step consists of filling the hole, which Gutierrez does teach. Alternatively, Gutierrez teaches the benefit of forming one selective tungsten plug on another regardless of the number of source gases, and the admitted prior art, like the instantly disclosed invention, does not disclose more than one source gas.

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Claims 1, 2, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view Gutierrez as applied to claim 9 above and further in view of Shioya [US 4,906,593], or Harada [US 5,128,278], or Nakata [US 5,071,789].

The admitted prior art in view of Gutierrez fail to disclose whether tungsten selectively deposited in a via or contact hole by CVD sticks out of the hole slightly. Nakata, Shioya, and Harada all teach that selective CVD tungsten (17, 5, and 26 respectively) when formed in a contact or via tends to stick out slightly (Figures 5b, 1b, and 3e, respectively). Hence, it would have been expected and unavoidable in the process of the admitted prior art in view of Gutierrez that the selectively formed CVD tungsten plug would have stuck out slightly as taught by Nakata, Shioya, and Harada.

Applicant's arguments filed 10/15/96 have been fully considered but they are not persuasive.

Applicant argues that since Guittierez teaches a tungsten deposition process where the source gases must be changed, Guittierez doesn't teach a single step deposition. However, for the reasons stated above in the rejection, the process of the admitted prior art in view of Guittierez does meet the limitations of the claimed invention.

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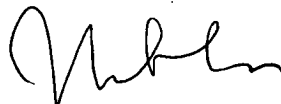
This office action has been created under the Patent and Trademark Office Semiconductor Technology Quality Assurance Pilot Program. It incorporates the examination quality standards set as a result of customer focus sessions with the semiconductor industry. The listing of the field of search to follow is one of these standards.

| Field of Search | Date |
|---|----------|
| U.S. Class and subclass: 437/189,190,195,195,981 | 10/31/96 |
| Other Documentation: | |
| Electronic data base(s): | |


Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Thomas Bilodeau whose telephone number is (703) 308-1090. The examiner can normally be reached on Monday through Friday from 6:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached on (703) 308-3325. The fax numbers for this group are (703)305-3599 and (703)305-3600.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0661.



John Niebling
Supervisory Primary Examiner
Art Unit 1107


Thomas Bilodeau
October 31, 1996